1	/18
2	/20
3	/17
4	/19
5	/16
6	/10

MASSACHUSETTS INSTITUTE OF TECHNOLOGY
DEPARTMENT OF ELECTRICAL ENGINEERING AND COMPUTER SCIENCE

6.191 Computation Structures
Spring 2025

Quiz #1

Name	*Athena login name*	*Score*

Recitation section

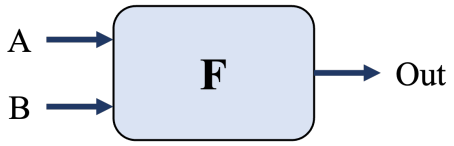
☐ WF 10, 34-302 (Hilary)	☐ WF 2, 34-302 (Raymond)	☐ WF 12, 35-308 (Keshav)
☐ WF 11, 34-302 (Hilary)	☐ WF 3, 34-302 (Raymond)	☐ WF 1, 35-308 (Keshav)
☐ WF 12, 34-302 (Ezra)	☐ WF 10, 35-308 (Harry)	☐ WF 2, 8-205 (Vedantha)
☐ WF 1, 34-302 (Ezra)	☐ WF 11, 35-308 (Harry)	☐ WF 3, 8-205 (Vedantha)
		☐ opt-out

Please enter your name, Athena login name, and recitation section above. Enter your answers in the spaces provided below. Show your work for potential partial credit. You can use the extra white space and the back of each page for scratch work.

Problem 1. Digital Abstraction (18 points)

The F module follows the voltage transfer characteristic given below. Assume that V_A and V_B are within the range of 0V to 6V, inclusive.

$$\mathbf{V_{out}} = \begin{cases} \mathbf{5.9V} & (\mathbf{V_A + 0.8 * V_B \leq 3.6V}) \\ \mathbf{1.0V} & (\mathbf{V_A + 0.8 * V_B > 3.6V}) \end{cases}$$



(A) (3 points) Given the above specification for module F, determine the Boolean expression that module F(A, B) implements. Express your answer in terms of A and B.

A	B	Out
0	0	1
0	1	0
1	0	0
1	1	0

If both inputs are 0V, out = 5.9V (high)

If V_A = 0V and V_B = 6V, Out = 1.0V (low)

If V_A = 6V and V_B = 0V, Out = 1.0V (low)

If V_A = 6V and V_B = 6V, Out = 1.0V (low)

This is a NOR gate.

Boolean Expression for F(A, B): Out = ____$\overline{A + B}$_____

(B) (5 points) Identify the signaling specification parameters, ($V_{OL}, V_{IL}, V_{IH}, V_{OH}$), that maximize both the low noise margin and the high noise margin for module F. Then provide the noise immunity for module F. You must show your work.

To maximize the low and high noise margin we want to set V_{OL} as low as possible and V_{OH} as high as possible. In addition, the circuit must be able to produce these output voltages. So we set them to the two output values produced by the circuit.

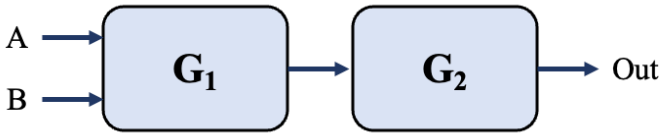
Since two low inputs must produce a high output, that means that for all low inputs $\mathbf{V_A + 0.8 * V_B \leq 3.6V}$. Since V_{IL} is the highest valid low input then $1.8V_{IL} \leq 3.6$. So $V_{IL} \leq 2$.

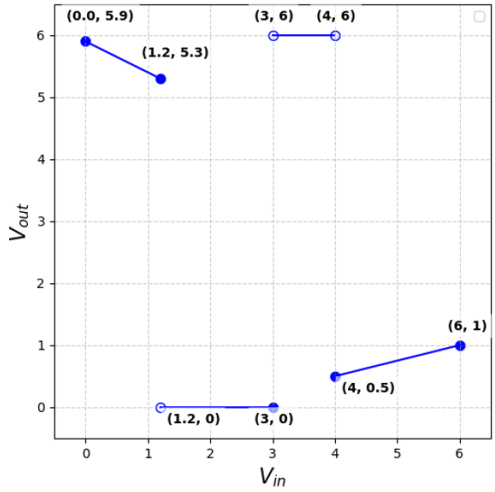
A low and high input or two high inputs must produce a low output. To produce a low output, $V_A + 0.8 * V_B > 3.6V$. The lowest V_{IH} that satisfies this equation occurs when $V_A = 0$, and $V_B = V_{IH}$ Thus $0.8V_{IH} > 3.6$. So $V_{IL} > 3.6/0.8 = 36/8 = 4.5V$.

V_{OL} = ___1.0V___ , V_{IL} = __2V___, V_{IH} = __4.5V___, V_{OH} = ___5.9V__

Noise Immunity: ____1V_____

The G module, which implements the same Boolean function as the F module, consists of two subcircuits G_1 and G_2. G_1 is either the $max(V_A, V_B)$ or $min(V_A, V_B)$. You will need to figure out which. G_2 follows the voltage transfer characteristic shown to the right below.





(C) (3 points) In order for G to implement the same Boolean function as F, which function of (V_A, V_B) should you use for G_1: $max(V_A, V_B)$ or $min(V_A, V_B)$? Explain why.

G_1 is (select one): $\mathbf{max(V_A, V_B)}$ $\mathbf{min(V_A, V_B)}$

Explanation:

In order for module G to behave like a NOR gate, it must produce a low output for the three combinations (0, 1) (1,0) and (1, 1). Since G_2 produces a low output when its Vin is high, we want G_1 to produce a high output for these three cases, so G_1 must be the max(V_A, V_B). Note that both functions produce a high output when both inputs are low.

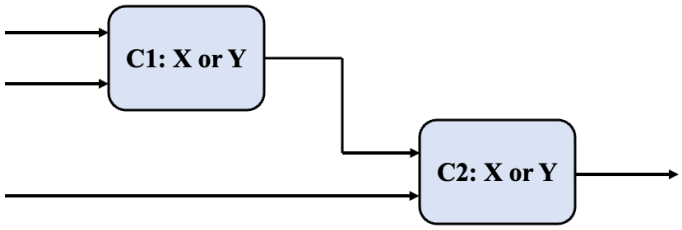
(D) (4 points) Identify the signaling specification parameters, ($V_{OL}, V_{IL}, V_{IH}, V_{OH}$), that maximize the noise immunity of G_2. Also, specify the resulting noise immunity.

The VTC shows us that for all $V_{in} < 1.2$, G_2 can produce a high output and for all $V_{in} > 4$ G_2 can produce a low output as long as we define a valid high to be 5.3V or higher and a valid low to be 1V or lower. So $V_{OL} = 1V$, $V_{IL} = 1.2V$, $V_{IH} = 4V$, and $V_{OH} = 5.3V$.

$\boldsymbol{V_{OL}}$ = __**1V**__ , $\boldsymbol{V_{IL}}$ = ___**1.2V**___ , $\boldsymbol{V_{IH}}$ = __**4V**__ , $\boldsymbol{V_{OH}}$ = __**5.3V**___

Noise Immunity: _____**0.2V**_____

(E) (3 points) Now consider two new modules, X and Y, which have the following signaling specification parameters: Module X ($V_{OL}, V_{IL}, V_{IH}, V_{OH}$) = (1V, 2V, 5V, 6V), module Y ($V_{OL}, V_{IL}, V_{IH}, V_{OH}$) = (0.5V, 1.5V, 4V, 4.5V). You want to combine one X module with one Y module as shown below. Determine whether the X module should be placed in the position labeled C1 or C2 assuming that Y will go in the other one, so that the resulting circuit behaves as a valid combinational device. Explain your answer.



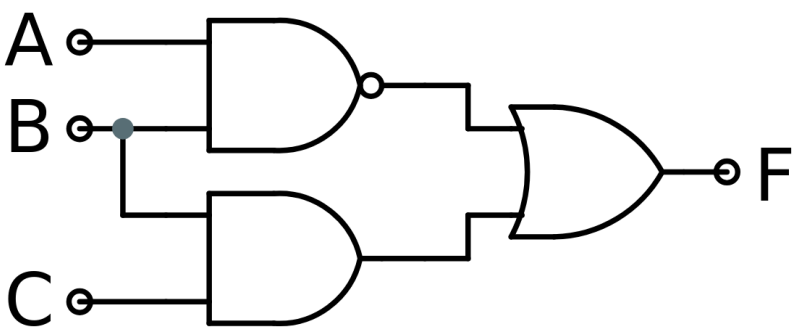
Placement of Module X : C1 / C2

Explanation:

C1 must produce valid input to C2. Based on the specifications for modules X and Y, a low output from X (1V) is a valid low input for Y (< 1.5V) and a high output for X (6V) is a valid high input for Y (>4V). On the other hand even though a low output from Y (0.5V) is a valid low input for X (<2V), a high output from Y (4.5V) is not a valid high input for X which requires a high input to be at least 5V.

Problem 2. Boolean Algebra (20 points)

(A) (3 points) Consider the following circuit that implements the Boolean expression $F(a,b,c) = \overline{ab} + bc$.



1. Fill in the truth table for expression F below.

a	b	c	F
0	0	0	**1**
0	0	1	**1**
0	1	0	**1**
0	1	1	**1**
1	0	0	**1**
1	0	1	**1**
1	1	0	**0**
1	1	1	**1**

2. What is a minimal sum-of-products expression for $F(a,b,c)$?

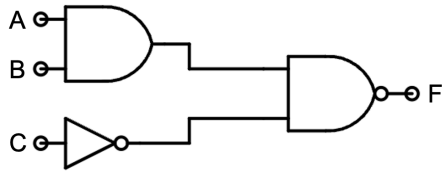
$\overline{a} + \overline{b} + bc$ (de morgans)

$\overline{a} + (\overline{b} + b)(\overline{b} + c)$ (distribute)

$\overline{a} + \overline{b} + c$ (reduction)

Minimal sum-of-products form for F = _____ $\overline{a} + \overline{b} + c$ _____

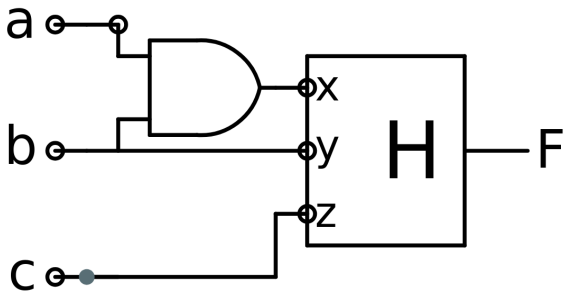
(B) (3 points) Oh no! Somehow you lost all of your OR gates! Draw a circuit implementation for F without using OR gates. **You may only use inverters and 2-input AND and NAND gates. Use the minimal number of gates for full points.**



$\overline{a} + \overline{b} + c = \overline{ab} + c = \overline{\overline{ab} + c} = \overline{\overline{ab}\,\overline{c}} = \overline{ab\overline{c}}$

This expression is equal to 1 AND, 1 NOT, and 1 NAND.

(C) (2 points) You found some OR gates, but in the process you accidentally dropped and ruined all your NAND gates! Luckily, you also found gate H, which implements the expression $H(x, y, z) = \overline{x} + yz$. It turns out you can still implement F by using an H gate. Using a **single** additional gate which can be an **inverter**, or a **2-input AND** gate, or a **2-input OR** gate, connect the inputs *a*, *b*, and *c* to the inputs of gate H to produce the function F. **Hint:** You may want to implement something other than the minimal sum of products for F.



(D) (2 points) Use Boolean algebra to demonstrate that your implementation of F out of H plus one gate, from part (C), is equivalent to F.

$H(ab, b, c) = \overline{ab} + bc = \overline{a} + \overline{b} + bc = \overline{a} + \overline{b} + c$

(E) (2 points) Determine whether the gate $H(x, y, z) = \overline{x} + yz$ is functionally complete (universal). If it is, prove it. Otherwise, explain why it is not.

$H(x, 0, 0) = \overline{x}$ (not)
$H(1, y, z) = yz$ (and)

H can be an AND and NOT gate, so it is universal

(F) (4 points) Find **a minimal sum-of-products** expression for each of the following Boolean expressions. **Pay close attention to which variables are under the overbars.** To get credit for your answer, you must **use Boolean algebra axioms and properties and show your work!**

1. $a\overline{cd} + \overline{b}cde + \overline{a}\,\overline{c}\,e + de$

   $a\overline{cd} + \overline{a}\,\overline{c}\,e + de$ absorption
   $a\overline{d} + a\overline{c} + \overline{a}\,\overline{c}\,e + de$ de morgans and distribute
   $a\overline{d} + \overline{c}(a + \overline{a}e) + de$ distribute
   $a\overline{d} + \overline{c}(a + e) + de$ distribute and identity
   $a\overline{d} + a\overline{c} + \overline{c}e + de$ distribute

2. $\overline{b(\,\overline{ac} + b)}\left(a\overline{b}c + \overline{a}\right)d$

   $\overline{b}\left(a\overline{b}c + \overline{a}\right)d$ absorption
   $\overline{b}\left((\overline{a} + a)\left(\overline{a} + \overline{b}c\right)\right)d$ distribute
   $\overline{b}\left(\overline{a} + \overline{b}c\right)d$ complements
   $\overline{a}\overline{b}d + \overline{b}cd$

(G) (4 points) Determine whether each of the Boolean expressions below are satisfiable. If it is satisfiable, give an input assignment that make the expression satisfiable. You must provide a valid value for each variable. If it is not satisfiable, show why it is not.

1. $\left(\overline{d + \overline{a}\overline{b}}\right)(ab + cd)(ad + d)$

right term simplifies to d, so d=1

if d=1, then left term must be 0 (left term implements NOR)

unsatisfiable

alternatively, can do the boolean algebra to reduce to 0

2. $(abc + \overline{d})(\overline{c} + a)\left(\overline{d + \overline{b}}\right)$

right term is NOR, so d=0 and b=1

if d=0 then left term = 1

middle term means c = 0 OR a = 1 (the only assignment that doesn't work is c=1 and a=0)

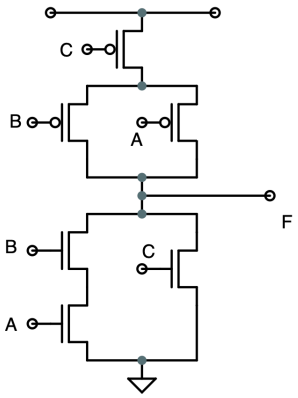
d=0, b=1, (a, c) = (0, 0) or (1, 0) or (1, 1)

Problem 3. CMOS Logic (17 points)

(A) (10 points) For each of the following four functions (specified as a Boolean expression or as a truth table), determine if it can be implemented as a single CMOS gate. If it can, draw the CMOS gate using a minimal number of FETs. If not, describe why it cannot be implemented as a single CMOS gate.

1. $F(A,B,C) = \bar{A}\bar{C} + A\bar{B}\bar{C}$

We can simplify this to $\bar{C}(\bar{A} + A\bar{B})$
Which we can then simplify to $\bar{C}(\bar{A} + \bar{B})$
Implementing this as a CMOS will take 3-nfets and 3-pfets. If we expanded this out to minimal SOP form we would get $\bar{C}\bar{A} + \bar{C}\bar{B}$ which takes 4-nfets and 4-pfets, so we choose not to expand this out. Drawing the CMOS we get:



2. $\overline{F(A,B,C,D)} = AB + \overline{CD}$

There is no way to simplify this expression to get rid of the $\bar{C}$, which means we cannot implement this as a single CMOS gate

3.

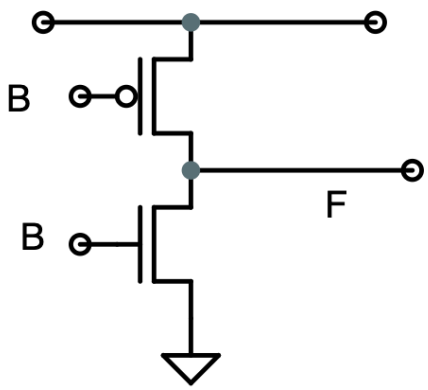
A	B	C	F
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

For a circuit to be implementable as a single CMOS gate, rising outputs must be accompanied by falling inputs and vice versa. However, the top two rows in the table have a rising output (F goes from 0 to 1), but no falling input to accompany it.

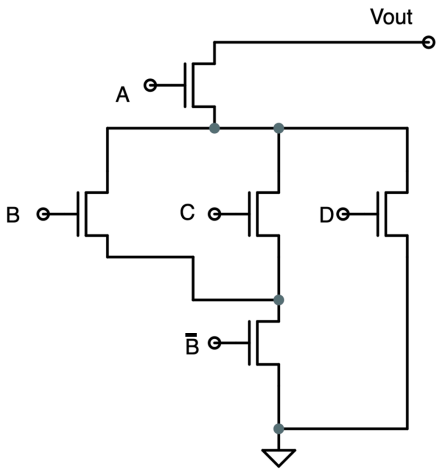
4.

A	B	C	F
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	0

We could convert this to normal form and simplify this. But instead we can also inspect the chart and realize $F = \bar{B}$, which means we can draw this quite simply:



(B) (2 points) Evaluate the output of the below circuit at the following points. We have only drawn the pull-down circuit. Assume the pullup is complementary. Notice that one of the inputs is connected to $\overline{B}$.



What is Vout when A=1, B=1, C=0, D=0? _____1_____

The pulldown is equivalent to an open circuit, so the pullup must be active

What is Vout when A=1, B=0, C=1, D=0? _____0_____

The pulldown successfully connects Vout to ground.

(C) (3 points) Given that a function $F(A, B, C)$ can be implemented as a single CMOS gate, complete the truth table below. For each row, enter a 0 or 1 if you can deduce the value of F for that set of inputs, and enter ? if you cannot.

A	B	C	F
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

F(0, 0, 0) must be 1 since if it was 0, then F(1, 1, 0) which is 1 will have a rising output w/out a falling input
F(1, 1, 1) must be 0 since if it was 1 then F(0, 0, 1) which is 0 will have a rising output w/out a falling input
F(0, 1, 1) must be 0 since if it was 1, then F(0, 0, 1) which is 0 will have a rising output w/out a falling input
F(0, 1, 0) must be 1 since if it was 0, then F(1, 1, 0) which is 1 has a rising output w/out a falling input

F(1, 0, 0) must be 1 since if it was 0, then F(1, 1, 0) which is 1 has a rising output w/out a falling input
F(1, 0, 1) must be 0, since if it was 1 then F(0, 0, 1) which his 0 has a rising output w/out a falling input

(D) (2 points) If some function G can **NOT** be implemented as a single CMOS gate, when can $\bar{G}$ be implemented as a single CMOS gate? Select one of the options and explain your answer. Use examples and/or counter examples in your explanation.

Always **Sometimes** **Never**

Explanation:

XOR and XNOR are both not implementable as a single CMOS gate.

AND is not implementable as a single CMOS gate, but NAND is implementable.

4. Combinational Minispec (19 points)

(A) (8 points) Complete the truth table for the following Minispec function.

```
function Bit#(3) f(Bit#(1) a, Bit#(2) b);
    Bit#(3) ret = 3'b100;
    case ({b[0], a})
        0: ret = {1'b1, zeroExtend(a) & b};
        1: ret = signExtend(a) + zeroExtend(b);
        3: ret = {~a, b};
        default: ret = 3'b110;
    endcase
    return ret;
endfunction
```

a	b[1]	b[0]	ret[2]	ret[1]	ret[0]
0	0	0	**1**	**0**	**0**
0	0	1	**1**	**1**	**0**
0	1	0	**1**	**0**	**0**
0	1	1	**1**	**1**	**0**
1	0	0	**1**	**1**	**1**
1	0	1	**0**	**0**	**1**
1	1	0	**0**	**0**	**1**
1	1	1	**0**	**1**	**1**

(B) (3 points) Below is an implementation of a parametric function `add_mod3#(n)` which takes two n-bit inputs `a` and `b` and returns a 2-bit output `(a+b) mod 3`.

```
function Bit#(2) add_mod3#(2) (Bit#(2) a, Bit#(2) b);
   Bit#(3) sum = zeroExtend(a) + zeroExtend(b);
   return truncate(sum % 3);
endfunction

function Bit#(2) add_mod3#(Integer n) (Bit#(n) a, Bit#(n) b);
   Bit#(2) r = 0;
   for(Integer i = 0; i < n; i = i + 2) begin
      Bit#(2) s = add_mod3#(2)(a[i+1:i], b[i+1:i]);
      r = add_mod3#(2)(r, s);
   end
   return r;
endfunction
```

The delay of this implementation of add_mod3#(n) in terms of n is Θ(____n _____)

Justification:

Each iteration of the for loop uses add_mod3#(2)(r, s) with an input r which is a result from the previous iteration. Because of this all these n/2 instances of add_mod3#(2) are chained together one after another and therefore the delay is O(n).

(C) (8 points) Implement a recursive version of `add_mod3#(n)` which achieves a better asymptotic delay. The base case `add_mod3#(2)` is provided for you. You can assume that `n` is a power of 2 and that $n \geq 2$. What is the delay of your implementation of `add_mod3#(n)`? Justify your answer.

```
function Bit#(2) add_mod3#(2) (Bit#(2) a, Bit#(2) b);
   Bit#(3) sum = zeroExtend(a) + zeroExtend(b);
   return truncate(sum % 3);
endfunction

function Bit#(2) add_mod3#(Integer n) (Bit#(n) a, Bit#(n) b);
   Bit#(2) s0 = add_mod3#(n/2)(a[n/2-1:0], b[n/2-1:0]);
   Bit#(2) s1 = add_mod3#(n/2)(a[n-1:n/2], b[n-1:n/2]);

   return add_mod3#(2)(s0, s1);




endfunction
```

The delay of your implementation of add_mod3#(n) in terms of n is Θ(____log(n)____)

Justification:

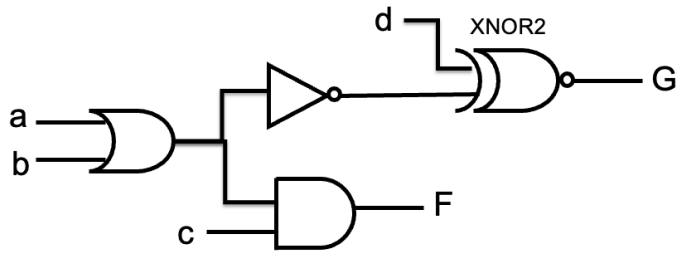
At each step of the recursion the computation is split between s0 and s1 such that they can be computed concurrently. Moreover, at each step n is divided by 2, so the depth of the recursion is $O(\log_2 n)$, and hence the delay of add_mod3#(n) is O(log(n)).

Problem 5. Combinational and Sequential Logic Timing (16 points)

Two 6.1910 students have built a circuit that sends them reminders to complete the lecture questions at 9:50am. They use a logic family with the following characteristics for their circuits (in *nanoseconds*):

Gate	t_{PD}	t_{CD}	t_{SETUP}	t_{HOLD}
AND2	1.7	0.4	—	—
OR2	1.8	0.3	—	—
XNOR2	2.1	0.2	—	—
INV1	0.5	0.3	—	—
REG	2.4	0.9	1.2	0.8

(A) (2 points) They initially design the combinational circuit below with two outputs, F and G. What are the t_{PD} and t_{CD} values of the combinational circuit?



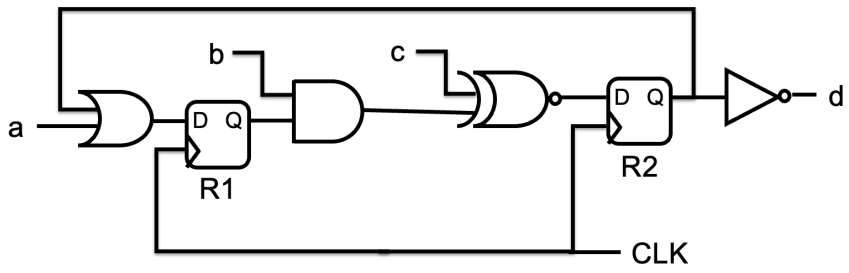
Path with the longest propagation delay is a/b → G: $t_{PD,OR2} + t_{PD,INV1} + t_{PD,XNOR2} = 1.8 + 0.5 + 2.1 = 4.4$

Path with the shortest contamination delay is d → G: $t_{CD,XNOR2} = 0.2$

t_{PD} (ns): _____4.4_____

t_{CD} (ns): _____0.2_____

(B) (4 points) They learn about sequential circuits and come up with the new circuit below. What is the minimum $\mathbf{t_{CLK}}$ value for which this circuit operates correctly? Write "N/A" if the circuit is not valid. For full credit, you must show that all setup and hold timing constraints are fully satisfied, or that one of the constraints is not satisfied.



R1 to R2:

$t_{CLK} \geq t_{PD,REG} + t_{PD,AND2} + t_{PD,XNOR2} + t_{SETUP,REG} = 2.4 + 1.7 + 2.1 + 1.2 = 7.4$

$t_{CD,REG} + t_{CD,AND2} + t_{CD,XNOR2} \geq t_{HOLD,REG} \rightarrow 0.9 + 0.4 + 0.2 = 1.5 \geq 0.8$

R2 to R1:

$t_{CLK} \geq t_{PD,REG} + t_{PD,OR2} + t_{SETUP,REG} = 2.4 + 1.8 + 1.2 = 5.4$

$t_{CD,REG} + t_{CD,OR2} \geq t_{HOLD,REG} \rightarrow 0.9 + 0.3 = 1.2 \geq 0.8$

Both hold constraints are satisfied

Minimum t_{CLK} (ns): _____7.4_____

(C) (2 points) What are the $\mathbf{t_{PD}}$ and $\mathbf{t_{CD}}$ values of the sequential circuit?

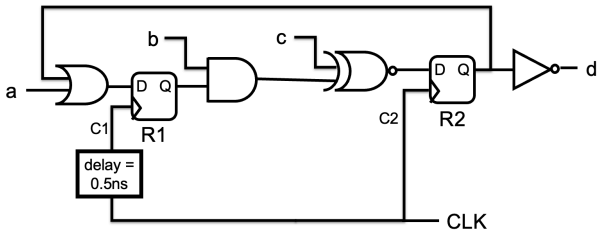
$t_{PD,REG} + t_{PD,INV1} = 2.4 + 0.5 = 2.9$

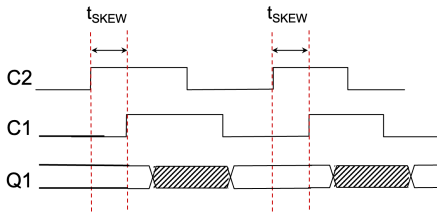
$t_{CD,REG} + t_{CD,INV1} = 0.9 + 0.3 = 1.2$

t_{PD} (ns): _____2.9_____

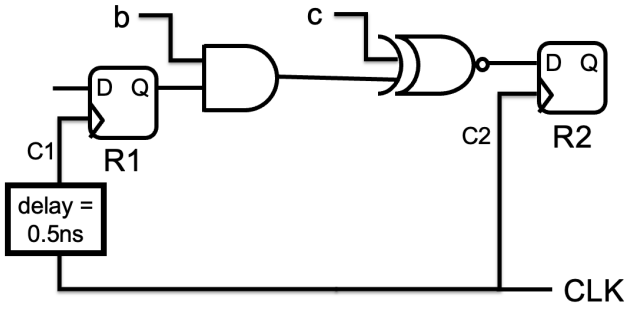
t_{CD} (ns): _____1.2_____

The students realize that because the CLK → R1 wire is much longer than the CLK → R1 wire, the clock signal does not arrive at R1 and R2 at the same time. As shown below, this circuit has clock skew where the CLK signal arrives at register R1 $\mathbf{t_{SKEW}}$ = 0.5ns after it arrives at register R2.





(D) (3 points) To ensure their circuit operates correctly, they remove some logic to focus only on the R1 → R2 path. What is the minimum $\mathbf{t_{CLK}}$ value for which this circuit operates correctly? Write "N/A" if the circuit is not valid. For full credit, you must show that all setup and hold timing constraints are fully satisfied, or that one of the constraints is not satisfied.



$t_{CLK} - t_{SKEW} \geq t_{PD,REG} + t_{PD,AND2} + t_{PD,XNOR2} + t_{SETUP,REG} = 2.4 + 1.7 + 2.1 + 1.2 = 7.4$

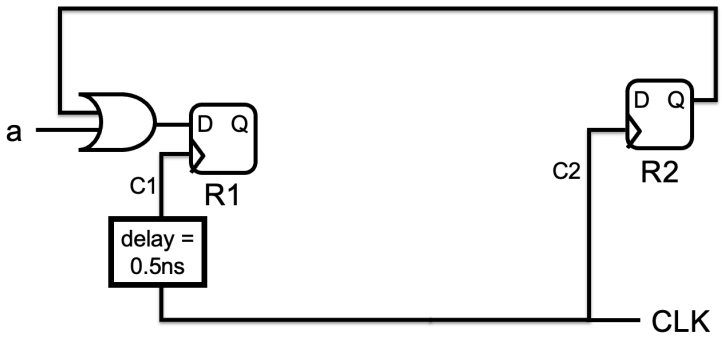
$t_{CLK} \geq 7.4 + 0.5 = 7.9$

$t_{CD,REG} + t_{CD,AND2} + t_{CD,XOR2} \geq t_{HOLD,REG} - t_{SKEW}$
$0.9 + 0.4 + 0.2 = 1.5 \geq 0.8 - 0.5 = 0.3$

The hold constraint is satisfied.

Minimum t_{CLK} (ns): _____7.9_____

(E) (2 points) They then analyze the R2 → R1 path by creating the simplified circuit below. What is the minimum t_{CLK} value for which this circuit operates correctly? Write "N/A" if the circuit is not valid. For full credit, you must show that all setup and hold timing constraints are fully satisfied, or that one of the constraints is not satisfied.



$t_{CLK} + t_{skew} \geq t_{PD,REG} + t_{PD,OR2} + t_{SETUP,REG} = 2.4 + 1.8 + 1.2 = 5.4$

$t_{CLK} \geq 5.4 - 0.5 = 4.9$

$t_{CD,REG} + t_{CD,OR2} \geq t_{HOLD,REG} + t_{skew}$ → $0.9 + 0.3 \geq 0.8 + 0.5$

$1.2 < 1.3$ so this hold time constraint is not satisfied.

Minimum t_{CLK} (ns): _____N/A_____

(F) (3 points) The students find new registers REGA and REGB that they consider substituting in for both R1 and R2 in their sequential circuit with clock skew. Which register should they use to ensure that their circuit operates correctly and minimizes the value of t_{CLK}? Circle which register type to select and explain why you should choose that register type.

Gate	t_{PD}	t_{CD}	t_{SETUP}	t_{HOLD}
REG	2.4	0.9	1.2	0.8
REGA	2.8	0.9	1.0	0.6
REGB	2.2	0.6	0.8	0.5

Circle one: **REG** **REGA** **REGB**

Explanation:

REG:
In part E, we already showed that the original REG does not satisfy the R2 → R1 hold time constraint.

REGA:
R1 → R2:
$t_{CD,REG} + t_{CD,AND2} + t_{CD,XOR2} \geq t_{HOLD,REG} - t_{SKEW}$
$0.9 + 0.4 + 0.2 = 1.5 \geq 0.6 - 0.5 = 0.1$

R2 → R1:
$t_{CD,REG} + t_{CD,OR2} \geq t_{HOLD,REG} + t_{skew}$
$0.9 + 0.3 = 1.2 \geq 0.6 + 0.5 = 1.1$

REGB:
R1 → R2:
$t_{CD,REG} + t_{CD,AND2} + t_{CD,XOR2} \geq t_{HOLD,REG} - t_{SKEW}$
$0.6 + 0.4 + 0.2 = 1.2 \geq 0.5 - 0.5 = 0$

R2 → R1:
$t_{CD,REG} + t_{CD,OR2} \geq t_{HOLD,REG} + t_{skew}$
$0.6 + 0.3 = 0.9 \geq 0.5 + 0.5 = 1.0$
This constraint is not satisfied.

REGA is the only register that can satisfy all of the hold time constraints.

Problem 6. A Variant Lock (10 points)

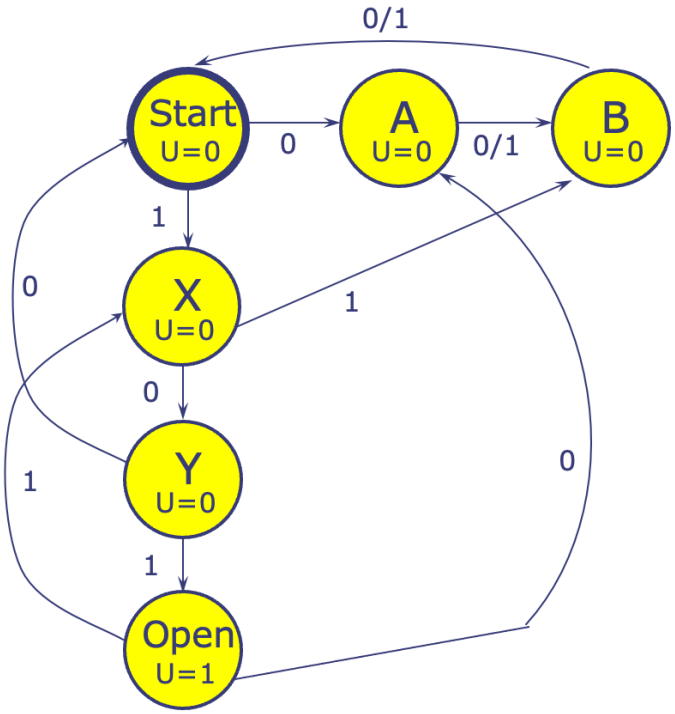
In lecture, we saw an example of a digital combination lock which was designed such that as long as the last 4 inputs were correct, then the lock would unlock. You are now tasked with designing a different type of lock which samples 3 inputs at a time and **resets** to its initial state every time you enter an invalid 3-input combination. This lock has the following specifications:

- It begins in the `Start` state.
- It receives a 1-bit input ("0" or "1") on every cycle
- It produces a 1-bit output ("Unlock" signal) on every cycle
- Inputs are sampled in groups of 3
- UNLOCK (U) is 1 if the sampled group of 3 inputs matched the "combination": 101, otherwise UNLOCK = 0.
- If the sampled group of 3 inputs did not match the combination, then go back to the Start state.

The following examples should clarify the expected operation of this lock:

- **Receive 101.** Lock opens. FSM reaches a state where Unlock=1 after receiving 3 bits.
- **Receive 1101.** FSM in non-Start state with Unlock = 0.
- **Receive 10001.** FSM in non-Start state with Unlock=0.
- **Receive 100100.** FSM back in start state with Unlock=0.
- **Receive 000101.** Lock opens.
- **Receive 101101.** Lock opens after 3rd bit, and then again after 6th bit.

(A) (10 points) Draw the state transition diagram for this combination lock. Your starting state should be labeled `Start`. Label all other states with a unique letter (e.g. X). Make sure to specify the value of the output U for each state. Also, make sure to label each transition with a 0, 1, or 0/1 (if arc can be followed for either a 0 or 1 input). Your FSM must handle all possible input combinations. For full credit, you should minimize the number of states used in your FSM. *The following page has been intentionally left blank in case you want more space to draw your FSM.*



END OF QUIZ 1!