1	/18
2	/18
3	/16
4	/15
5	/18
6	/15

M A S S A C H U S E T T S   I N S T I T U T E   O F   T E C H N O L O G Y

DEPARTMENT OF ELECTRICAL ENGINEERING AND COMPUTER SCIENCE

**6.191 Computation Structures**

Fall 2023

Quiz #1

Name	Athena login name	Score

Recitation section

|		
☐ WF 10, 34-301 (Wendy)	☐ WF 2, 34-303 (Jessica)	☐ WF 12, 36-155 (Joey)
☐ WF 11, 34-301 (Wendy)	☐ WF 3, 34-303 (Jessica)	☐ WF 1, 36-155 (Joey)
☐ WF 12, 35-310 (Rona)	☐ WF 10, 34-302 (Helen)	☐ WF 1, 34-303 (Catherine)
☐ WF 1, 35-308 (Rona)	☐ WF 11, 36-112 (Helen)	☐ WF 2, 34-304 (Catherine)
		☐ opt-out

Please enter your name, Athena login name, and recitation section above. Enter your answers in the spaces provided below. Show your work for potential partial credit. You can use the extra white space and the back of each page for scratch work.

Problem 1. The Digital Abstraction (18 points)

Device **F** has the following digital voltage thresholds and voltage transfer curve.
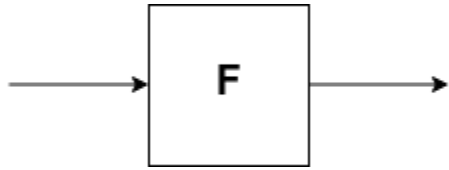
- $V_{OL} = 0.1V_{DD}$
- $V_{IL} = 0.2V_{DD}$
- $V_{IH} = 4$
- $V_{OH} = 0.8V_{DD}$
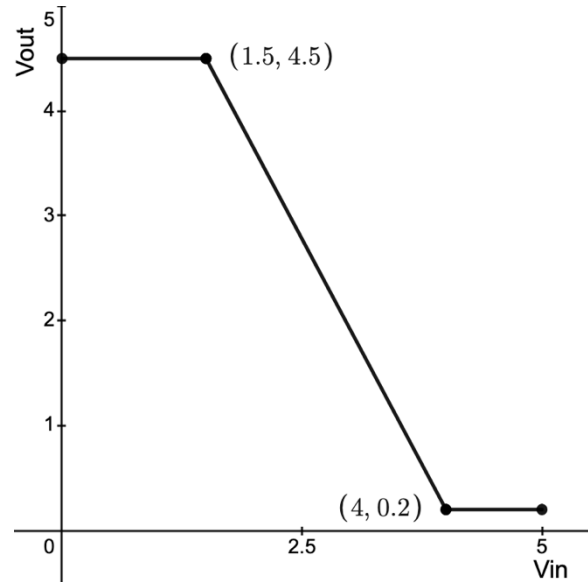
(A) (2 points) You are told that if $\mathbf{V_{DD}} = \mathbf{1\ V}$ ($V_{OL} = 0.1V$, $V_{IL} = 0.2V$, $V_{IH} = 4V$, $V_{OH} = 0.8V$), then F is invalid because it does not operate as a valid digital inverter with positive noise margins. Based on your understanding of the static discipline, provide **two** reasons to explain why this V_{DD} does not produce a valid inverter.

(B) (6 points) Now consider the following additional values of V_{DD}. For each value, determine whether **F** is *valid* (i.e. it can function as a valid digital inverter with positive noise margins). If **YES**, then write the noise immunity for **F**. Otherwise, write **INVALID** and briefly explain your reasoning. Note that the thresholds for each value of V_{DD} have been computed for you and are shown in parentheses.

    i. $V_{DD} = 4.5$ **V** ($V_{OL} = 0.45V$, $V_{IL} = 0.9V$, $V_{IH} = 4V$, $V_{OH} = 3.6V$)
        Noise immunity or INVALID? _____
        Brief explanation:

    ii. $V_{DD} = 5.5$ **V** ($V_{OL} = 0.55V$, $V_{IL} = 1.1V$, $V_{IH} = 4V$, $V_{OH} = 4.4V$)
        Noise immunity or INVALID? _____
        Brief explanation:

    iii. $V_{DD} = 6$ **V** ($V_{OL} = 0.6V$, $V_{IL} = 1.2V$, $V_{IH} = 4V$, $V_{OH} = 4.8V$)
        Noise immunity or INVALID? _____
        Brief explanation:

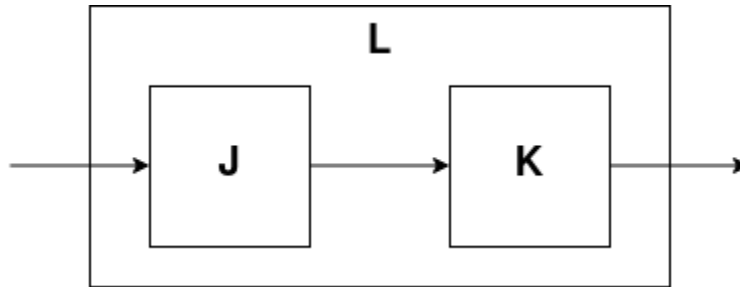(C) (3 points) For what range of values for V_{DD}, if any, is **F** *valid* (i.e., has noise immunity > 0)?

You set **F** aside and move on to devices **J** and **K**. You find the following voltage thresholds for **J** and **K**.

- $V_{OL,J} = 0.6$
- $V_{IL,J} = 2.5$
- $V_{IH,J} = 3$
- $V_{OH,J} = 4.5$

- $V_{OL,K} = ???$
- $V_{IL,K} = ???$
- $V_{IH,K} = ???$
- $V_{OH,K} = ???$

You combine **J** and **K** into one functioning device, which you call **L.**

(D) (2 points) First let's check that device **K** accepts the outputs from **J**. Provide expressions for the constraints on $V_{IL,K}$ and $V_{IH,K}$ in terms of the voltage thresholds of **J** to ensure that outputs of **J** will be valid inputs to **K**. Also provide an expression for the noise immunity of the connection between **J** and **K**.

Constraint on $V_{IL,K}$ in terms of J thresholds: _____

Constraint on $V_{IH,K}$ in terms of J thresholds: _____

Noise Immunity of connection between J and K: _____

(E) (3 points) Now provide an expression for the voltage thresholds and noise immunity of the device **L** in terms of $V_{OL,K}$, $V_{IL,K}$, $V_{IH,K}$, and $V_{OH,K}$ and the J thresholds given above. You may assume that the noise immunity of the wire between **J** and **K** is large enough that it won't affect the voltage thresholds or noise immunity of **L**.

$V_{OL,L}$: _____   **$V_{IL,L}$:** _____   **$V_{IH,L}$:** _____   **$V_{OH,L}$:** _____

Noise Immunity of L: _____

(F) (2 points) We've finally found the voltage thresholds for device **K**.

- $V_{OL,K} = 0.2V_{DD}$
- $V_{IL,K} = 2$
- $V_{IH,K} = 3.1$
- $V_{OH,K} = 0.8V_{DD}$

Given these constraints, find the value of V_{DD} that maximizes the noise immunity of **L**.

V_DD: _____

Problem 2. Boolean Algebra (18 points)

(A) (4 points) Matthew has been given the task of implementing a Boolean function for Queen Frog's annual census of her domain. The function F takes in three Boolean variables, x, y, z and returns:

$$F(x, y, z) = \overline{xy + z} + \overline{yz + x} + xy\bar{z}$$

Fill in the truth table below. Then find the normal form and a minimal sum-of-products expression for $F(x, y, z)$.

x	y	z	F
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

1. **Normal form for F =** _____

2. **Minimal sum of products for F =** _____

(B) (3 points) Draw the circuit that implements F **using 3 or fewer gates**. You **may only use inverters and 2-input OR, NOR, AND,** and **NAND** gates in your circuit.

(C) (3 points) Queen Frog is delighted with Matthew and appoints him Head of the Census. She then asks him to construct all possible Boolean functions using only F gates and constants, which are the only gates she has available. Determine whether F is universal or not. Explain your answer. (F is included again below for your convenience.)

$$F(x, y, z) = \overline{xy + z} + \overline{yz + x} + xy\bar{z}$$

(D) (8 points) Matthew performs so well that Queen Frog assigns him even more Boolean expressions to simplify! Help Matthew by **finding a minimal sum-of-products** expression for each of the following Boolean expressions. Make sure your answer is in minimal-sum-of products form.

1. $a + \overline{(\bar{a} + \bar{b})(c + b)}$

2. $b(\bar{a} + c) + a(\bar{c} + b)(c + b)$

3. $a + b\bar{a} + c + \bar{a}\bar{b}\bar{c}$

4. $\left(a + \overline{bc}\right)\left(a + \overline{\bar{b} + \bar{c}}\right) + abc$

Problem 3. CMOS Logic (16 points)

Ben was scrolling on TikTok instead of paying attention to the CMOS lecture, so when he implemented his CMOS circuit below, the VTC he got *for some input values* is the one shown in Figure 1. It doesn't look right to him, but he can't quite figure out what's wrong with it either.
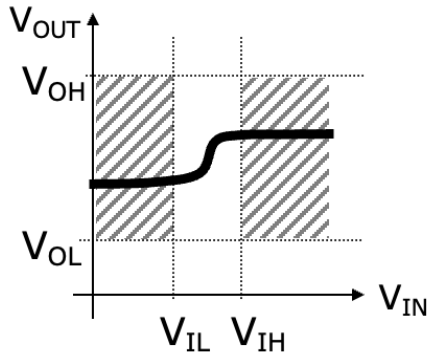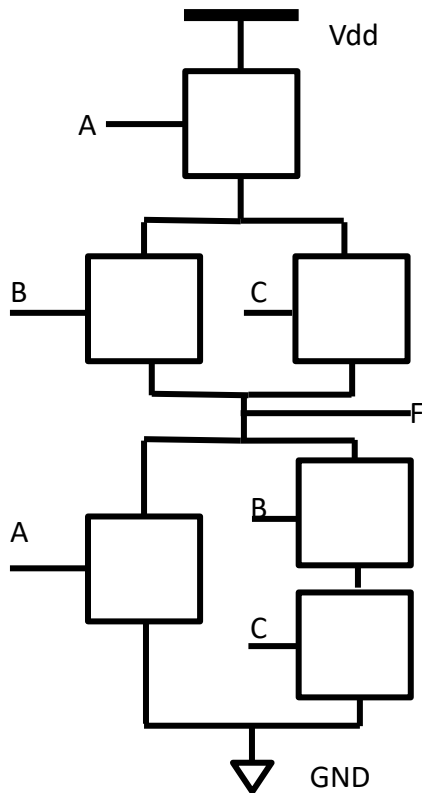

Figure 1: The initial VTC of Ben's circuit.

(A) (2 points) Help Ben figure out what's wrong with his circuit by labeling each blank box of his CMOS diagram as an nFET or a pFET, such that they correspond to the VTC he is getting.

(B) (3 points) Why does the VTC curve look like that?
Hint: note that valid inputs are leading to invalid outputs.

(C) (5 points) Now design a correct CMOS diagram that implements the function above, but does not have the issues Ben experienced with his design, i.e., valid and stable inputs should lead to valid and stable outputs. Once again, label each box as an nFET or pFET. Then, provide a Boolean expression for this function F in terms of A, B, and C.
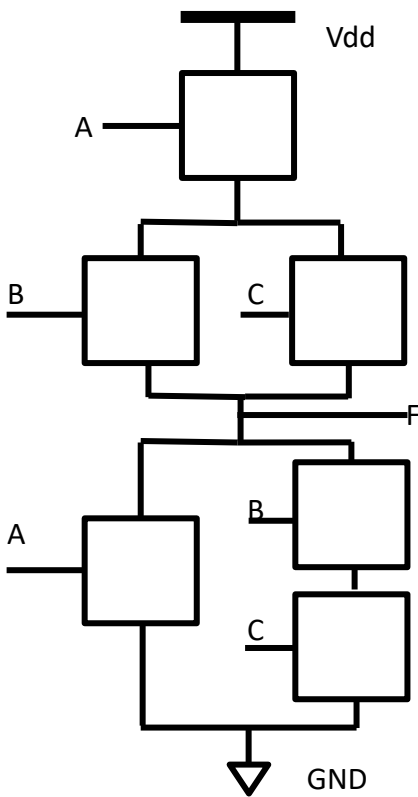
Boolean expression for F(A, B, C): _____

(D) (3 points) What does the new VTC curve look like for the same inputs as the one shown in Figure 1? (approximate shape is ok)
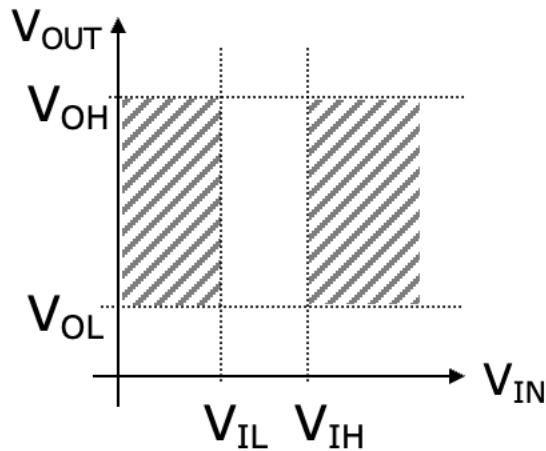
(E) (3 points) **Ben has now invented a new CMOS gate G** that implements a function described by the truth table below. However, he once again became distracted with TikTok and didn't notice that he copied the truth table for his gate G (Figure 2) incorrectly. He does, however, know that he has put an extra 1 where a 0 should have been.

Please correct the truth table by replacing the appropriate 1 with a 0 and explain why it was incorrect.
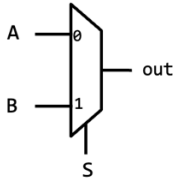
A	B	C	G
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	0

Figure 2: Truth table for Ben's circuit.

Explanation:

Problem 4. Combinational Circuits (15 points)

A 1-bit 2-to-1 mux takes in inputs A, B, S and outputs A if S is 0, and B if S is 1.

out = A·$\overline{\text{S}}$ + B·S

(A) (1 point) Draw a circuit that implements a 2-to-1 1-bit mux using only inverters and 2-input OR and AND gates. Make sure to clearly label all inputs and outputs.

(B) (2 points) Draw a circuit that implements a 2-to-1 1-bit mux using only 2-input NAND gates. Make sure to clearly label all inputs and outputs. For full credit, use **no more than 4 gates**.
Hint: how could you build an INV with only a single NAND gate?

Similarly, we can also build N-to-1 muxes, which take in N inputs, and a $\log_2(N)$-bit selector. Below is an example of a 4-to-1 mux.
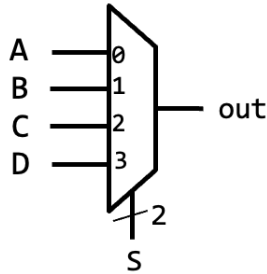
S[1]	S[0]	out
0	0	A
0	1	B
1	0	C
1	1	D

(C) (2 points) Write a minimal sum of products expression for the output out of a 1-bit 4-to-1 mux based on the inputs A, B, C, D, S[1], and S[0].

Minimal sum of products for out = _____

(D) (2 points) Draw a circuit that implements a 4-to-1 mux using only 2-to-1 muxes. Make sure to clearly label all inputs and outputs as well as the select value corresponding to each input.

(E) (8 points) Write a parametric function that implements a 1-bit N-to-1 mux using recursion, where N is a power of 2 (and N ≥ 2). You may represent the N 1-bit inputs as a single N-bit input `in`. This effectively is an nth bit selector. The base case function has been provided for you.

```
function Bit#(1) mux#(2)(Bit#(2) in, Bit#(1) sel);

    return (sel == 0) ? in[0]:in[1];

endfunction

function Bit#(1) mux#(Integer n)(Bit#(n) in, Bit#(log2(n)) sel);




















endfunction
```

Problem 5. Sequential Circuit Timing (18 points)

(A) (4 points) For each of the following circuits, determine if it is a valid combinational circuit and if so provide its propagation and contamination delays, otherwise label it as invalid. Assume that each gate has a t_{cd} of 1 ns and a t_{pd} of 2 ns.

i.
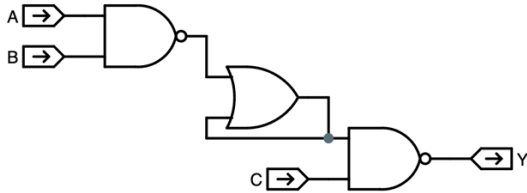
t_{cd} (ns) or Invalid: _____

t_{pd} (ns) or Invalid: _____

ii.

t_{cd} (ns) or Invalid: _____

t_{pd} (ns) or Invalid: _____

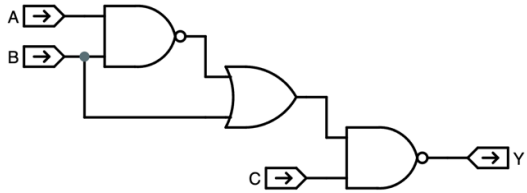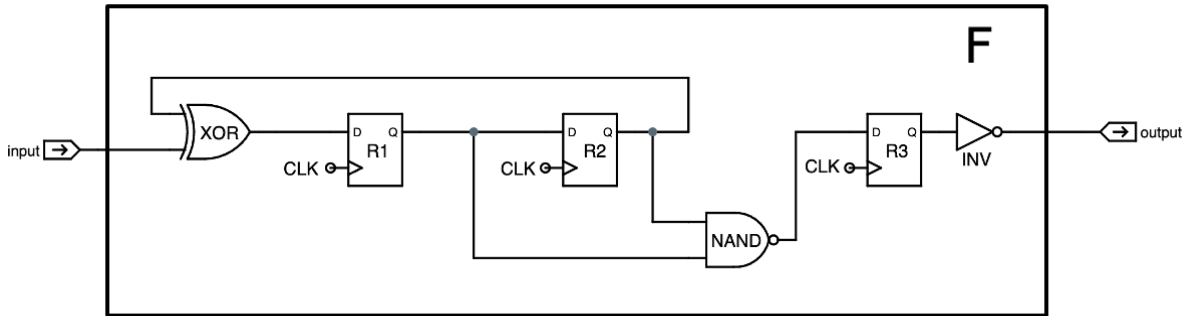Next, consider the following sequential circuit, F, with the timing constraints specified in the table below.

F

input → XOR → D Q R1 (CLK) → D Q R2 (CLK) → D Q R3 (CLK) → INV → output

NAND

Component	t_{pd} (ns)	t_{cd} (ns)	t_{hold} (ns)	t_{setup} (ns)
R1	1	0.5	0	1
R2	2	1	?	1.5
R3	3	2	?	2
XOR	5	1	--	--
NAND	2	1.5	--	--
INV	1	0.5	--	--

(B) (4 points) Provide maximum values for t_{hold} for registers R2 and R3 that will make this circuit operate as a valid sequential circuit.

$t_{hold,R2}$ (ns): _____

$t_{hold,R3}$ (ns): _____

(C) (3 points) Assuming valid values for $t_{hold,R2}$ and $t_{hold,R3}$, specify the minimum clock period for this circuit. Show your work.

$t_{clk,F}$ (ns): _____

(D) (4 points) What are the contamination delay and propagation delay of circuit F?

$t_{cd,F}$ (ns): _____

$t_{pd,F}$ (ns): _____

(E) (3 points) You now, want to connect two F components back to back as shown below so that the output of the first F module becomes the input to the second F module. What are the clock period, contamination delay, and propagation delay of this combined circuit, FF? Show your work.
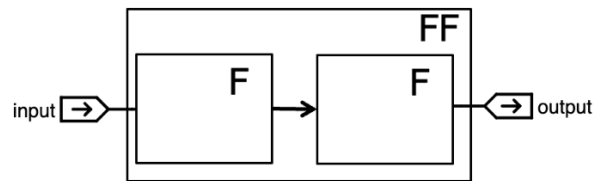
$t_{clk,FF}$ (ns): _____

$t_{cd,FF}$ (ns): _____

$t_{pd,FF}$ (ns): _____

Problem 6. Seasons Finite State Machine (15 points)
Consider the following finite state machine. The initial state is Spring.

(A) (3 points) Complete the truth table for this FSM below.

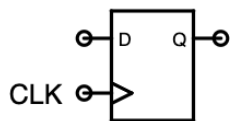| Current State	input	Next State	output
Spring	0	Summer	0
Spring	1	Fall	0
Summer	0	Winter	1
Summer	1	Fall	1
Fall	0	Fall	0
Fall	1	Winter	0
Winter	0	Spring	1
Winter	1	Winter	1

(B) (1 point) How many flip flops are needed to implement this FSM?

Number of flip flops: _____

(C) (3 points) Given the following inputs, determine the next state after the entire input has been processed. Assume that our FSM starts at the initial state for all inputs. Assume that the inputs are processed from left to right.

    i.   10000001   Next State: _____

    ii.   010111111000   Next State: _____

    iii.   010000001100011111111111   Next State: _____
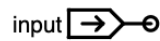
(D) (4 points) For the following input sequence, determine the current state, next state, and output for each cycle. Assume we start at the initial state, Spring, in cycle 1.

Cycle	1	2	3	4	5	6	7	8
Current State	Spring							
Input	1	0	0	1	1	1	1	0
Next State								
Output								

(E) (4 points) Consider a new FSM with the following truth table. Complete the circuit below to implement this FSM.

Current State	input	Next State	output
0	0	0	1
0	1	1	1
1	0	1	0
1	1	0	0

input →o

o→ output

D   Q
CLK o▷

END OF QUIZ 1!